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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/538,012	03/29/2000	Carole Dulong	42390.P6156	6257

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EXAMINER

WALTER, CRAIG E

ART UNIT

PAPER NUMBER

2188

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/538,012	<b>Applicant(s)</b> DULONG, CAROLE	
	<b>Examiner</b> Craig E. Walter	<b>Art Unit</b> 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 22 September 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 9/22/05 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 22 September 2005 has been entered.

### **Response to Amendment**

2. Applicant's arguments and amendments filed on 22 September 2005 in response to the office action mailed on 21 April 2005 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

3. The amended drawings (i.e. Fig. 9) filed on 22 September 2005 are deemed acceptable to the Examiner.

### **Response to Arguments**

4. Applicant's main argument that Austin's use of an address adder 103 with inputs, (which is used to add an increment value 101 and a start address 52) is limited in calculating an address until all previous addresses are incremented is

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not commensurate with the claim limitation as presented in amended claims (1, 8 and 14) of the pending application. Austin's disclosure does in fact teach adding a base address (start address 52) with an index (increment value 101) as claimed by applicant. The fact that Austin teaches adding *statically* valued indices (i.e. a fixed count value), which are further used to calculate each subsequent memory address (i.e. the fifth address cannot be calculated until the first four are calculated) is immaterial, as his disclosure still meets the limitations of the claims by "adding [each] said base address to each index".

### ***Claim Objections***

5. Claims 3, 10 and 16 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

As for claim 3, the limitation "computing addresses comprises adding each of said indices to a base address" is included as a limitation in claim 1.

As for claim 10, the limitation "calculating addresses comprises adding each of said indices to a base address" is included as a limitation in claim 8.

As for claim 16, the limitation “[the] processor computes addresses by adding each of said indices to a base address” is included as a limitation in claim 14.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 8-11, 14-17 and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Austin et al., hereinafter Austin (US Patent 3,163,850).

Referring to claim 1, Austin has taught a method for performing a gather operation on a general Purpose Computer processor comprising:

computing addresses for a plurality of data elements of a matrix stored in a memory wherein:

each data element is identified by one of an equal plurality of indices and a base address (Austin column 1, line 25 - column 2, line 50, column 5, lines 49-70, and figure 1, address adder 103 with inputs: increment value 101 and start address 52); and

computing addresses comprises executing an equal plurality of EXTRACT instructions to transfer a plurality of

said indices from a first storage location where the indices are stored substantially contiguously, to an equal plurality of separate storage locations, wherein each index is assigned its own separate storage location (Austin column 1, line 25 - column 2, line 50; column 5, lines 49-70; and figure 1, address adder 103 with inputs: increment value 101 and start address 52); and

adding said base address to each index (Austin column 5, lines 62-70 and figure 1, address adder 103 and start address 52 which acts as a base address.);

retrieving each of said plurality of data elements from memory based on the computed addresses (Austin column 5, lines 49-73); and

executing an equal plurality of DEPOSIT instructions, each deposit instruction depositing one or more of said data elements contiguously with other data elements in a general purpose register (Austin column 5, lines 49-73).

Further, it can be seen from Austin column 1, lines 10-24, column 2, lines 56-57 and column 6, lines 40-42 that Austin expressly discloses the scattering RSV instruction while not fully disclosing the details of the gathering RGV instruction since it is simply the inverse of the fully disclosed scattering RSV instruction.

Referring to claims 2 and 15, Austin has taught the method and the computer system wherein said storage locations are general purpose

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registers within a general purpose processor (Austin column 1, lines 25-35, column 5, lines 49-73 and figure 1, elements 19, 52, 75. It should also be noted that the basic data storage unit is a register, and would inherently be used to store these data elements).

Referring to claims 3 and 16, Austin has taught the method and the computer system wherein computing addresses further comprises adding each of said indices to a base address (Austin column 5, lines 62-70 and figure 1, address adder 103 and start address 52 which acts as a base address.).

Referring to claims 4 and 17, Austin has taught the method and the computer system further comprising loading each of said data elements from memory into separate storage locations prior to executing said second plurality of instructions (Austin column 2, lines 51-57, column 5, lines 49-70. Further, it can be seen from Austin column 2, lines 56-57 and column 6, lines 40-42 that Austin expressly discloses the scattering RSV instruction while not fully disclosing the details of the gathering RGV instruction since it is simply the inverse of the fully disclosed scattering RSV instruction.).

Referring to claim 8, Austin has taught a method for performing a scatter operation on a general Purpose Computer processor comprising:

executing a first plurality of EXTRACT instructions to extract indices for each of a plurality of data elements, the indices being extracted into separate storage locations (Austin column 5, lines

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49-73, specifically lines 62-70; and figure 1, increment value 101 acting as a calculated index;

using the extracted indices to calculate addresses in memory to which said plurality of data elements are to be scattered to form a matrix in memory wherein each address in memory is identified by one of a plurality of indices and a base address, and further wherein each address in memory is calculated by adding said base address to each index of said plurality of indices; (Austin column 1, line 25 - column 2, line 50; column 5, lines 49-70; and figure 1, address adder 103 with inputs: increment value 101 and start address 52 – also, column 5, lines 62-70 and figure 1, address adder 103 and start address 52, which acts as a base address.);

executing a second plurality of EXTRACT instructions, each of said EXTRACT instructions extracting one or more of said data elements from a separate storage location in which said data elements are stored contiguously to an equal plurality of separate storage locations (Austin column 5, lines 49-73 where Austin's RSV instruction corresponds to applicant's EXTRACT instruction and can be performed multiple times.); and

transferring said data elements from said separate storage locations to said calculated addresses in memory (Austin column 5, lines 49-73).

Referring to claim 9, Austin has taught the method wherein each of said storage locations is a general purpose register (Austin column 1, lines 25-35, column 5, lines 49-73 and figure 1, elements 19, 52, 75. It should also be noted that the basic data storage unit is a register and would inherently be used to store these data elements).

Referring to claim 10, Austin has taught the method wherein calculating addresses comprises adding each of said indices to a base address (Austin column 5, lines 62-70 and figure 1, address adder 103 and start address 52, which acts as a base address.).

Referring to claim 11, Austin has taught the method wherein storing each of said data elements is accomplished via a plurality of STORE instructions executed by said computer processor (Austin column 5, lines 49-55 where Austin's RSV instruction corresponds to applicant's EXTRACT instruction.).

Referring to claim 14, Austin has taught a computer system comprising:

- a memory (Austin figure 1, memory 16);

- a general purpose processor communicatively coupled to the memory (Austin figure 1, all elements beside memory 16 comprise the processor; and

- a storage device communicatively coupled to the processor and having stored therein a sequence of instructions (Austin figure

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1, memory 16 and column 1, lines 10-35) which, when executed by the processor, causes the processor to at least,

compute addresses for a plurality of data elements of a matrix stored in memory wherein:

each data element is identified by one of a plurality of indices and a base address (Austin column 1, line 25 - column 2, line 56; column 5, lines 49-70; and figure 1, address adder 103 with inputs: increment value 101 and start address 52); and

computing addresses comprises:

executing an equal plurality of EXTRACT instructions to transfer a plurality of said indices from a first storage location where the indices are stored substantially contiguously, to an equal plurality of separate storage locations, wherein each index is assigned its own separate storage location (Austin column 1, line 25 - column 2, line 50., column 5, lines 49-70.; and figure 1, address adder 103 with inputs: increment value 101 and start address 52); and

adding said base address to each index (Austin column 5, lines 62-70 and figure 1, address adder 103 and start address 52, which acts as a base address.);

retrieve each of said plurality of data elements from memory based on the computed addresses (Austin column 5, lines 49-73); and

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execute an equal plurality of DEPOSIT instructions, each deposit instruction to deposit one or more of said data elements contiguously with other data elements in a general purpose register (Austin column 5, lines 49-73).

Referring to claim 21, Austin has taught the method wherein computing addresses comprises executing a series of instructions, each instruction to extract an address index for one of said plurality of data elements (Austin column 5, lines 71-73 where execution of the instruction is repeated until address computation is complete.).

Referring to claim 22, Austin has taught the method wherein said address indices are extracted from a series of contiguous memory locations (Austin column 5, lines 49-70 where Austin's RSV scatter instruction takes a contiguous set of memory and scatters it to a discontinuous set of memory.).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 5, 7, 12-13, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Austin.

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Referring to claims 5, 12, and 18, Austin has not disclosed the method nor the computer system wherein said computer processor executes two or more of said first and/or second plurality of instructions in a single clock cycle. However, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to implement this scatter method in a modern superscalar computer system having an IPC (instructions per clock) of less than 1.

One of ordinary skill in the art would have been motivated to do this in order to have a faster and more efficient processing system.

Examiner takes Official Notice (see MPEP section 2144.03) that ("superscalar computing" in a computing environment was well known in the art at the time the invention was made. The Applicant is entitled to traverse any/all official notice taken in this action according to MPEP section 2144.03. However, MPEP section 2144.03 further states "See also *In re Boon*, 439 F.2d 724, 169 USPQ 231 (CCPA 1971) (a challenge to the taking of judicial notice must contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial notice)." Specifically, *In re Boon*, 169 USPQ 231, 234 states "as we held in *Ahlert*, an applicant must be given the opportunity to challenge either the correctness of the fact asserted or the notoriety or reputation of the reference cited in support of the assertion. We did not mean to imply by this statement that a bald challenge, with nothing more, would be all that was needed". Further note that 37 CFR section 671(c)(3) states "Judicial notice means official notice". Thus, a traversal by the Applicant that is merely "a bald challenge, with nothing more" will be given very little weight.

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Referring to claims 7, 13, and 20, Austin has not disclosed the method, nor the computer system wherein said registers are 64-bits wide and said data elements are 16-bits in length. However, at the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to store data elements of 16-bits length in 64-bit wide registers, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

8. Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Austin as applied to claims 1 and 14 above, and in further view of McDonnell et al., hereinafter McDonnell (US Patent 2,968,027).

Referring to claims 6 and 19, McDonnell has taught the method and the computer system further comprising storing each of said data elements on a mass storage device (McDonnell column 7, lines 23-28 and figure 1a, tape units 1-6). At the time the invention was made, it would have been obvious to a person of ordinary skill in the-art to include a mass storage device as McDonnell has disclosed in the gather-scatter system Austin has disclosed. A person of ordinary skill in the art would have found it obvious to use a more modern mass storage device - such as a hard disk etc. - as opposed to McDonnell's tape units. One of ordinary skill in the art would have been motivated to incorporate this portion of McDonnell's system into Austin's system because Austin repeatedly points a reader of his patent to McDonnell's system as the basis of his system

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(Austin column 1, lines 19-24, column 2, lines 33-38 and 45-46, column 3, lines 56-57).

### ***Conclusion***

9. This is a Request for Continued Examination (RCE) of applicant's earlier Application No. 09/538012. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. More specifically, the limitations added to the independent claims were present in dependent form during the previous action. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

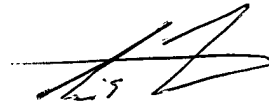
10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

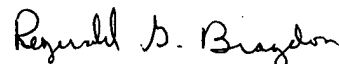
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Craig E Walter  
Examiner  
Art Unit 2188

CEW



REGINALD G. BRAGDON  
PRIMARY EXAMINER